Technical Specification for Multibus Interface

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1 Introduction

1.1 Overview

One of the most important elements in a computer system is the bus structure that supplies the interface for all the hardware components. This bus structure contains the necessary signals to allow the various system components to interact with each other. It allows memory and I/O data transfers, direct memory access.

iWave Systems has introduced multi bus interface which can be implemented on FPGA. It supports the following features:

1.2 Features

- Multi bus interface at 10MHz.
- Generic 16-bit CPU Interface
- Interrupt Generation.

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
FPGA	Field Programmable Gate Array
CPU	Central processing unit
ROM	Read only memory
SRAM	Static random access memory
EBUSC	External bus controller

2 CPU Interface to MULTIBUS

2.1 Logic Symbol

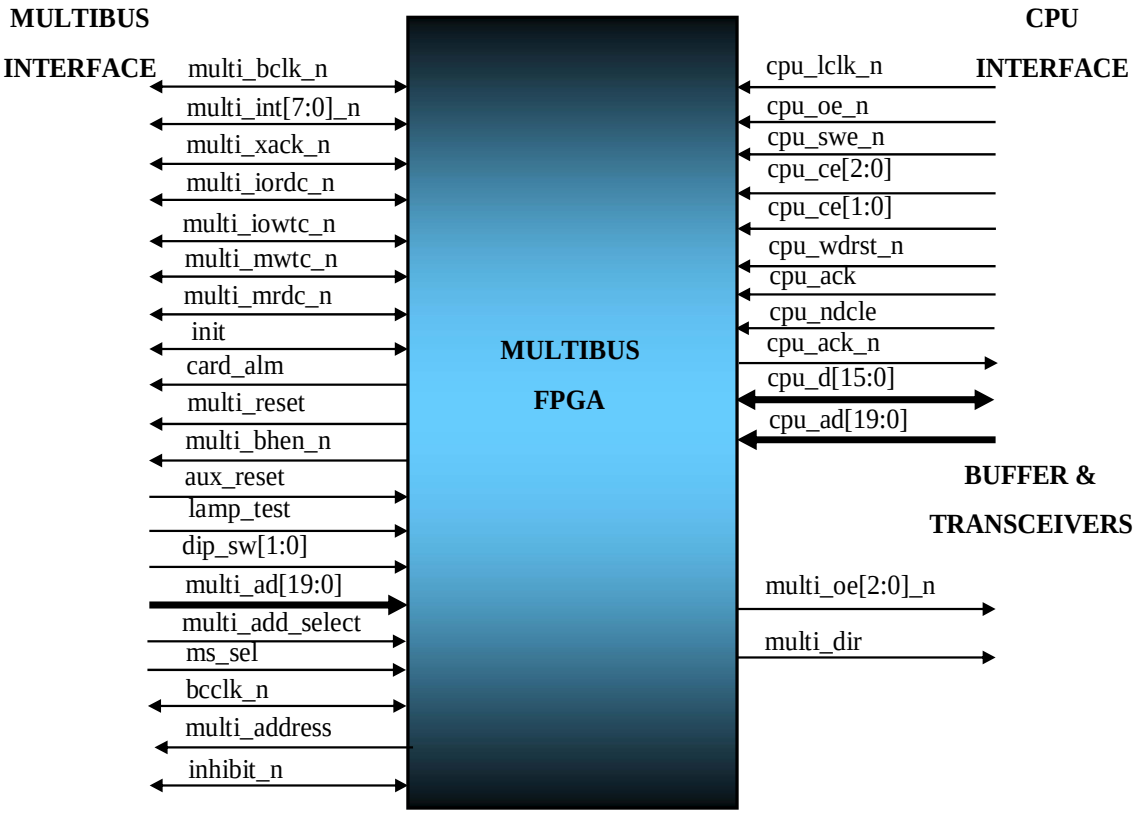

Figure 1 : CPU Interface to MULTIBUS

2.2 System Level Block Diagram

The FPGA in the Multibus Communication board is used to interface the external interface signals of the processor with the Multibus interface. The Multibus can be configured as the Master/Slave mode using the DIP switches connected to the FPGA.

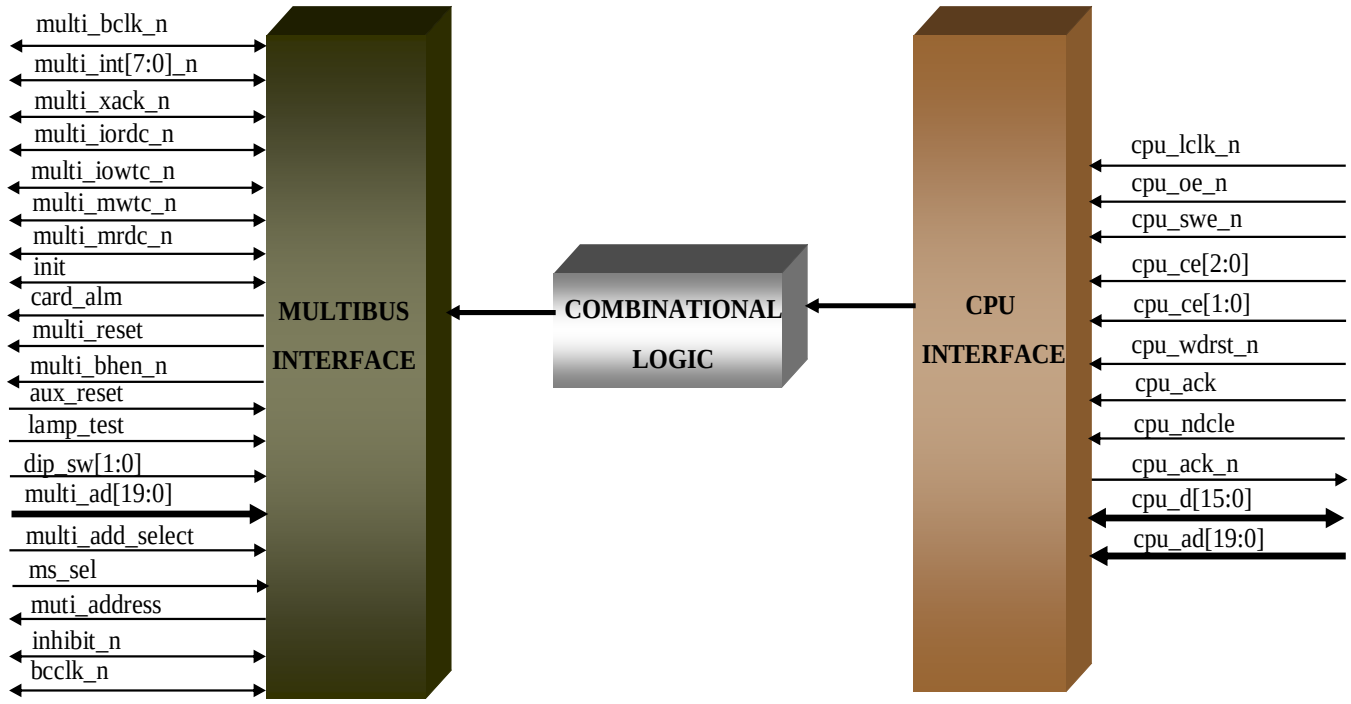

Figure 2 : System Level Block

2.3 CPU Interface

The CPU interface responds to the transactions from the CPU Interface. The external interface of the processor is connected. When the CPU is the bus master, then the memory/IO transactions from the processor interface are passed to the Multibus Interface.

2.4 Multibus Interface

The signals towards the Multibus side are generated by this interface. When the CPU is the bus master the processor interface signals are directly passed to Multibus side. When the CPU is the slave, the signals from the Multibus are input to the FPGA.

2.5 I/O Description

The I/O signals of the FPGA are described below.

2.5.1 System Interface Signal Description

Table 2 : multi bus Interface Signals

SIGNAL NAME	I/O	No of PINS	DESCRIPTION
multi_bclk_n	I/O	1	BUS CLOCK: A periodic signal used to synchronize the bus contention logic.
multi_ad[19:0]_n	I/O	20	ADDRESS LINES: These lines, which specify the address of the referenced memory location or I/O device.
multi_mrdc_n	I/O	1	MEMORY READ: The transition of the command indicates that the master has received the data from the source
multi_iordc_n	I/O	1	IO READ: Indicates that the I/O port address is valid on the address line and read operation is carried on
multi_iowtc_n	I/O	1	IO WRITE: Indicates that the I/O port address is valid on the address line and write operation is carried on
multi_mwtc_n	I/O	1	MEMORY WRITE: The active command line indicates that the data is valid on the bus and write operation is carried
multi_int[7:0]_n	I/O	8	INTERRUPT : This signals are used to request a interrupt
multi_init_n	I/O	1	INTIALIZE:This signal is used to initialize
multi_xack_n	I/O	1	ACKNOWLEDGE LINE: This command indicates to the master that the requested action is complete and the data has been placed on, or accepted from, the data lines
card_alarm	O	1	CARD ALARM: used for card alarm function

SIGNAL NAME	I/O	No of PINS	DESCRIPTION
multi_bhen_n	O	1	BYTE HIGH ENABLE: Used in 16 bit mode to indicate higher order bits are used
ms_sel	I	1	MASTER/SLAVE SELECT: Used to select master or Slave configuration.
multi_add_select	I	1	ADDRESS SELECTON : Used to select address selection
lamp_test	I	1	LAMP TEST : Used for lamp test function
aux_reset	I	1	AUXILARY RESET: Provides auxiliary reset function
bcclk_n	I/O	1	Multibus Constant Clock signal
inhibit_n	I/O	1	Multibus Slave Inhibit signal
multi_address	O	1	Multibus address output

2.5.2 Buffers & Transceivers Interface Signals

Table 3 : Buffers & Transceivers Interface Signals

SIGNAL NAME	I/O	No of PINS	DESCRIPTION
multi_dir	O	1	MULTIBUS DIRECTION: To control the direction between Multibus Interface and Processor
multi_oe[2:0]	O	3	MULTIBUS OUTPUT ENABLE: To enable the buffers between Multibus interface and processor

2.5.3 CPU Interface Signals

Table 4 : CPU Interface Signals

SIGNAL NAME	I/O	No of PINS	DESCRIPTION
cpu_ce[2:0]	I	3	CHIP ENABLE: Chip select signals for ROM, SRAM, and I/O devices
cpu_be[1:0]	I	2	BYTE ENABLE: Indicates a valid position on the data bus during read and write operation
cpu_ad[20:0]	I	20	ADDRESS LINES: Used to send address signals
cpu_lclk	I	1	SYSTEM CLOCK: Clock for external devices
cpu_oe_n	I	1	OUTPUT ENABLE: Used as output enable signal for ROM, RAM and I/O devices
cpu_ace	I	1	ADDRESS CLOCK ENABLE: Latch enable signal for the high order address bits of ADDR
cpu_ack_n	O	1	DATA ACKNOWLEDGE/READY: Cpu flow control signal
cpu_d[19:0]	I/O	16	DATA LINES: This signals are used to send and receive data
cpu_swe_n	I	1	WRITE ENABLE: Write enable for processor
cpu_wdrst_n	I	1	WATCHDOG RESET: Watchdog reset signal

3 Waveforms

3.1 EBUSC Timing

3.1.1 EBUSC Write waveform

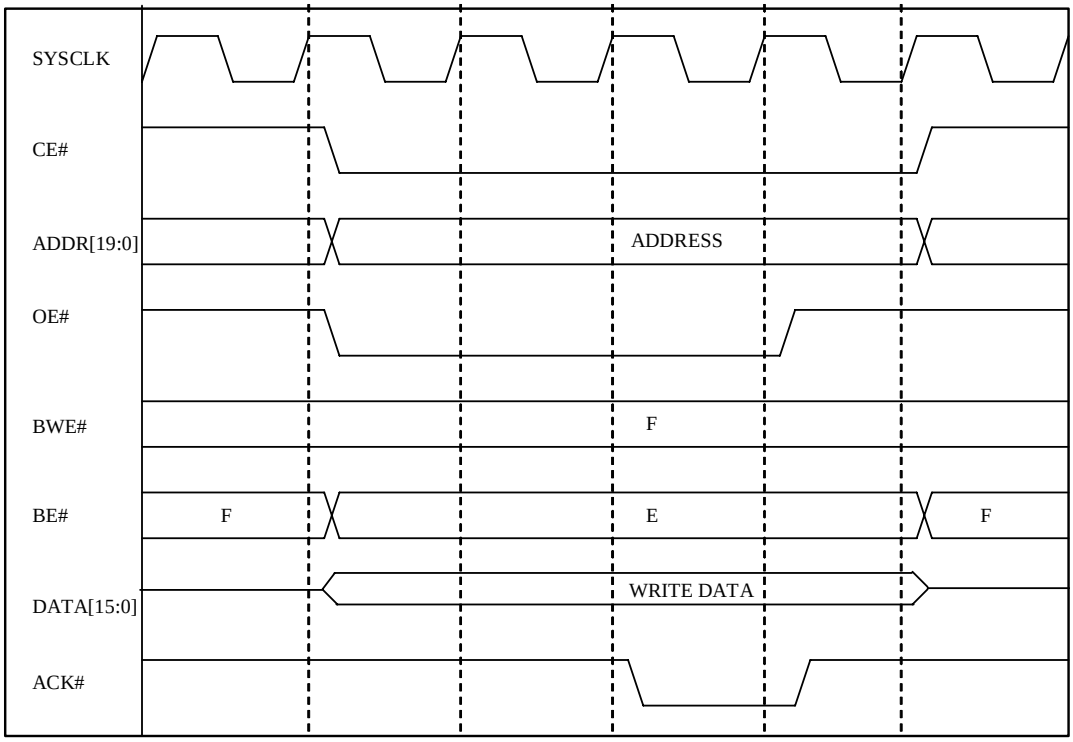

Figure 3 : EBUSC write Waveform

3.1.2 EBUSC Read waveform

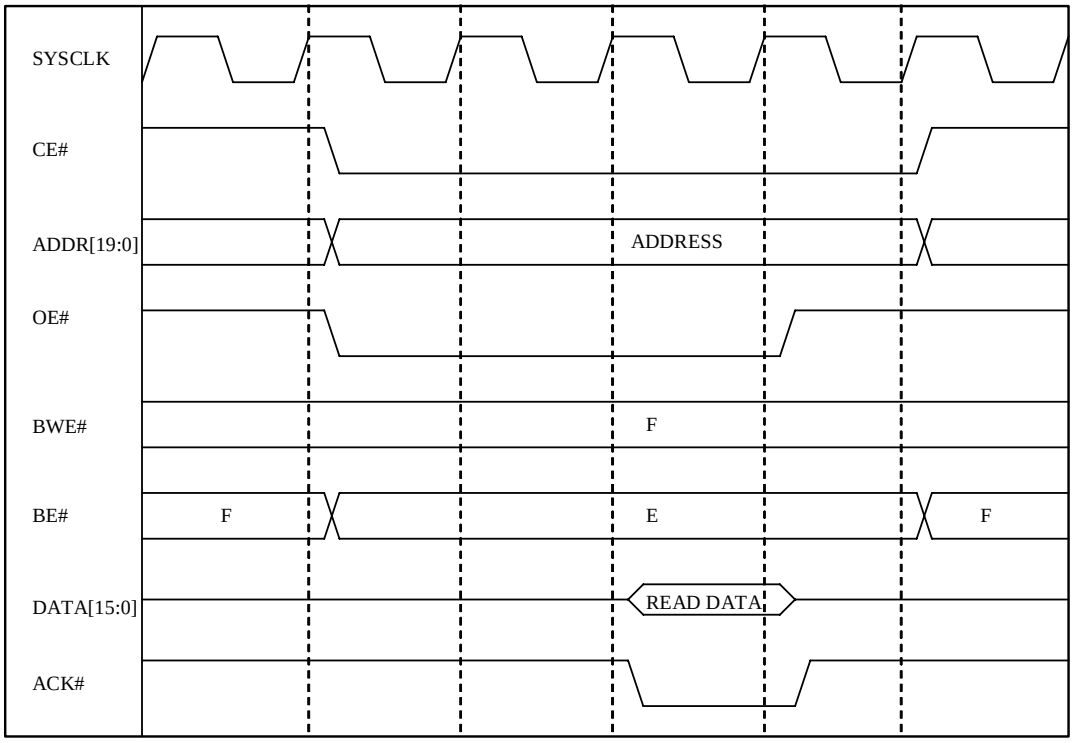

Figure 4 : EBUSC read Waveform

3.2 Multi bus Waveforms

3.2.1 Multibus Write Timing Waveform

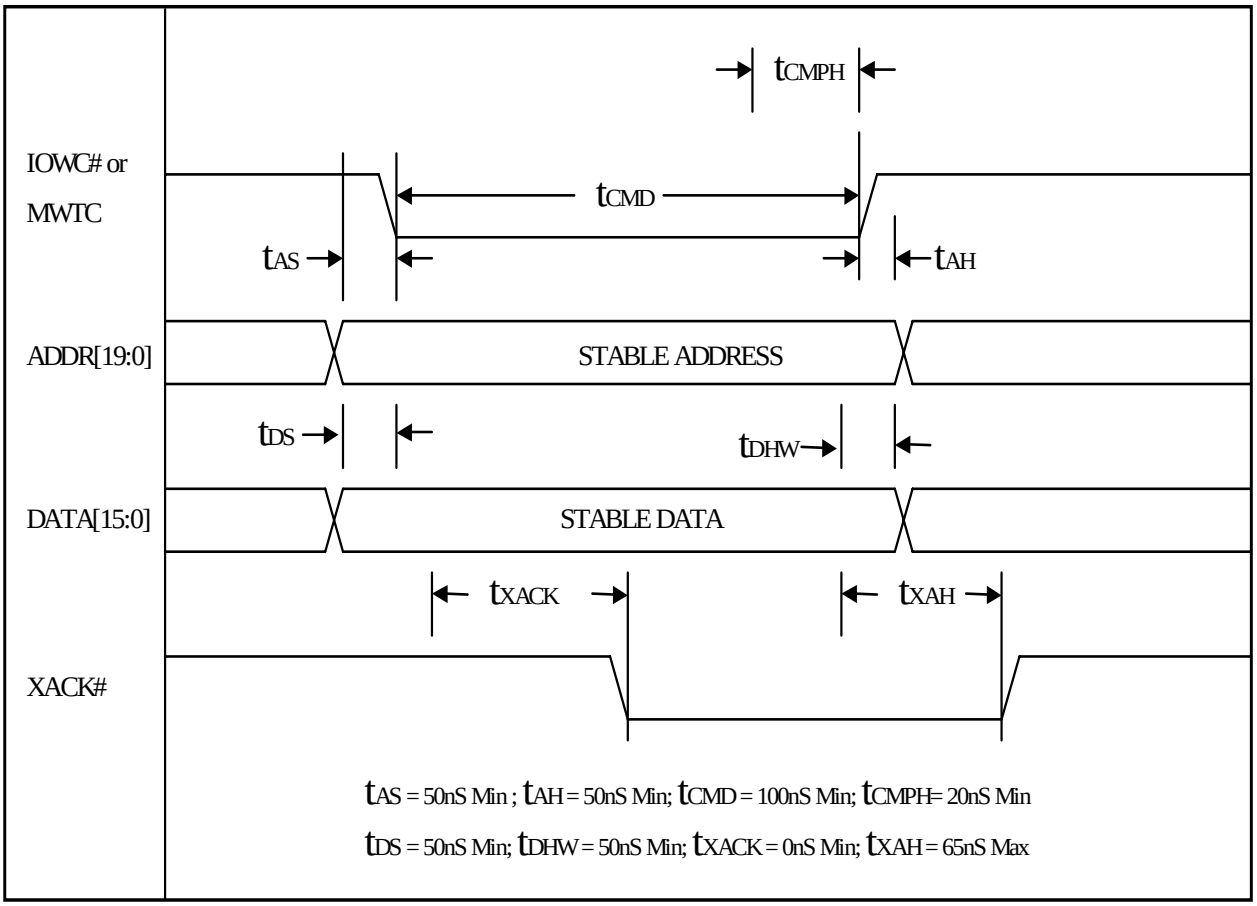

Figure 5 : Multibus Write waveform

3.2.2 Multibus Read Timing Waveform

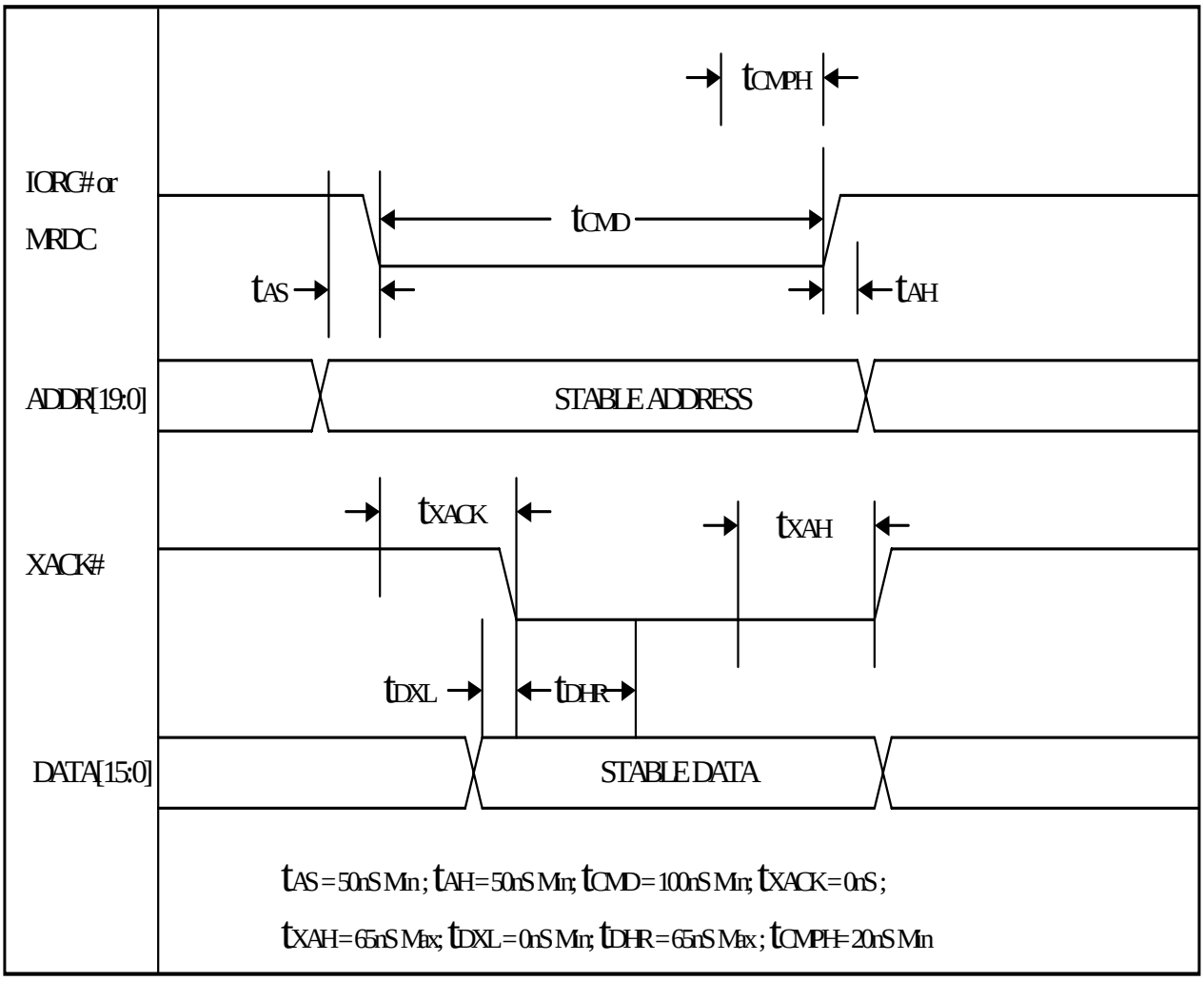

Figure 6: Multibus Read Timing